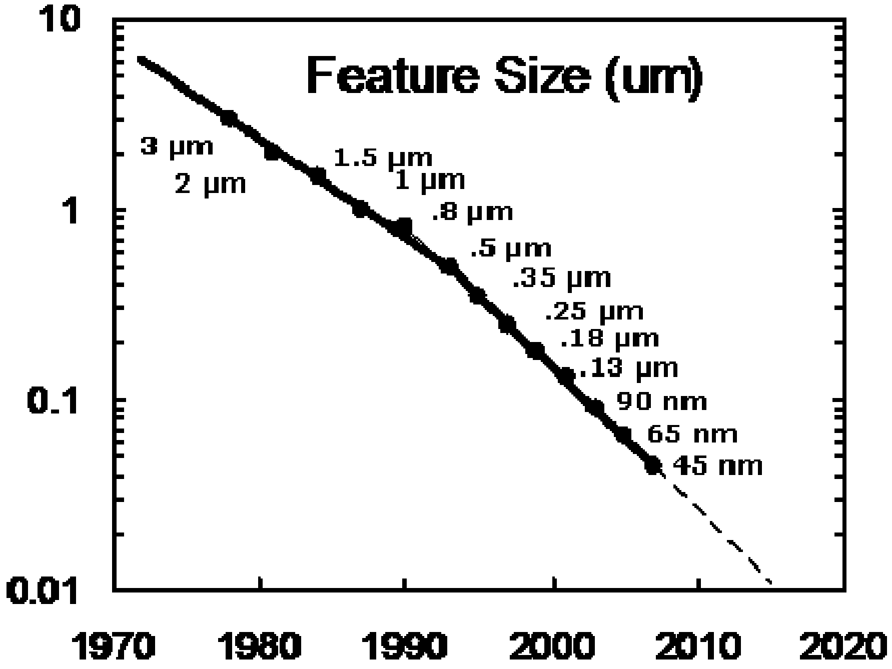
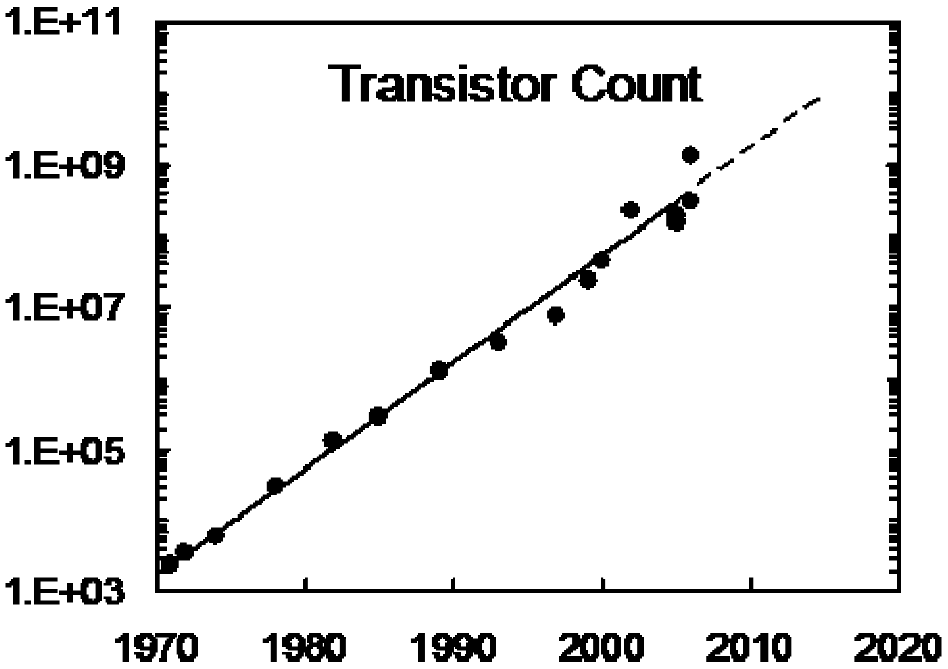
LithoVision | 2009

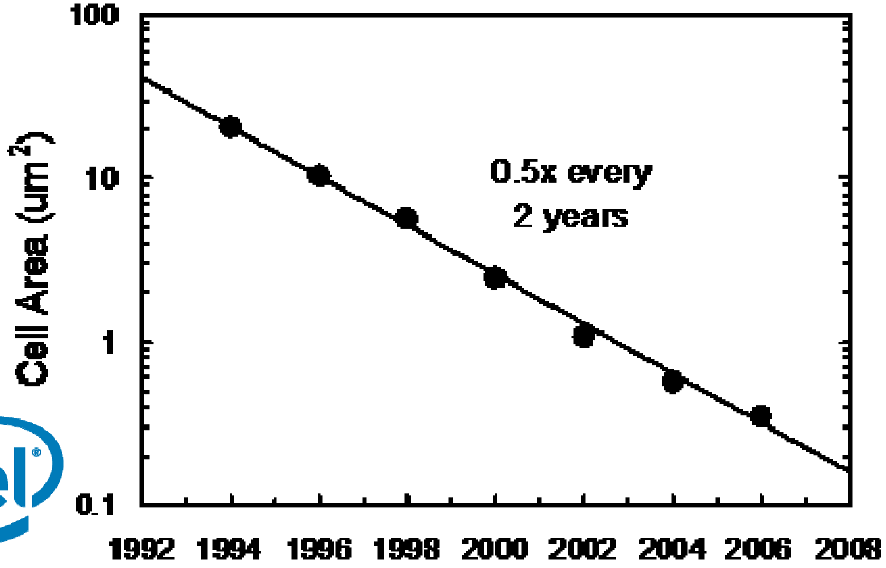
Lithography Technology Trends

Sam Sivakumar
Intel Corporation

Moore’s Law at Intel



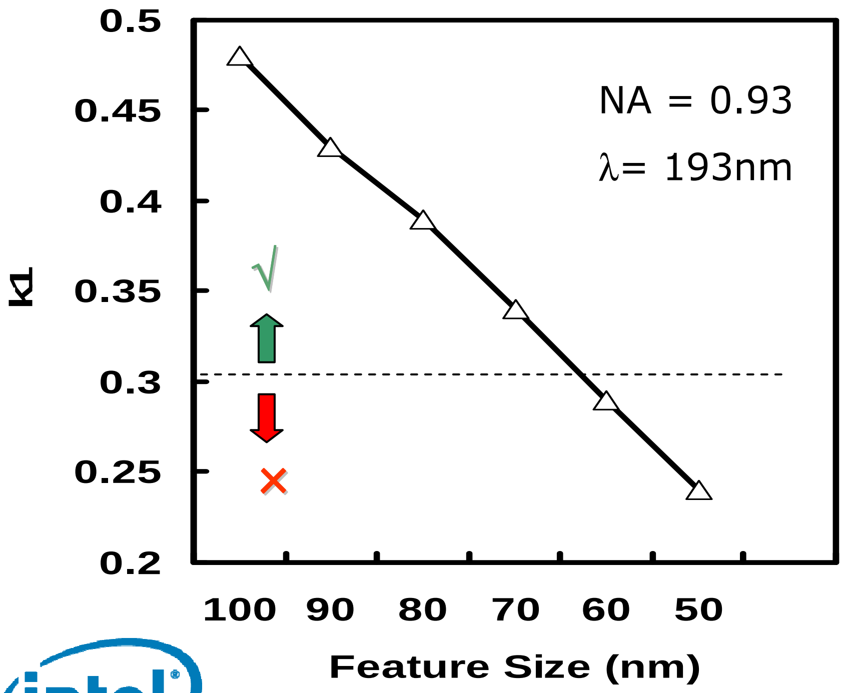




We expect the trend to continue

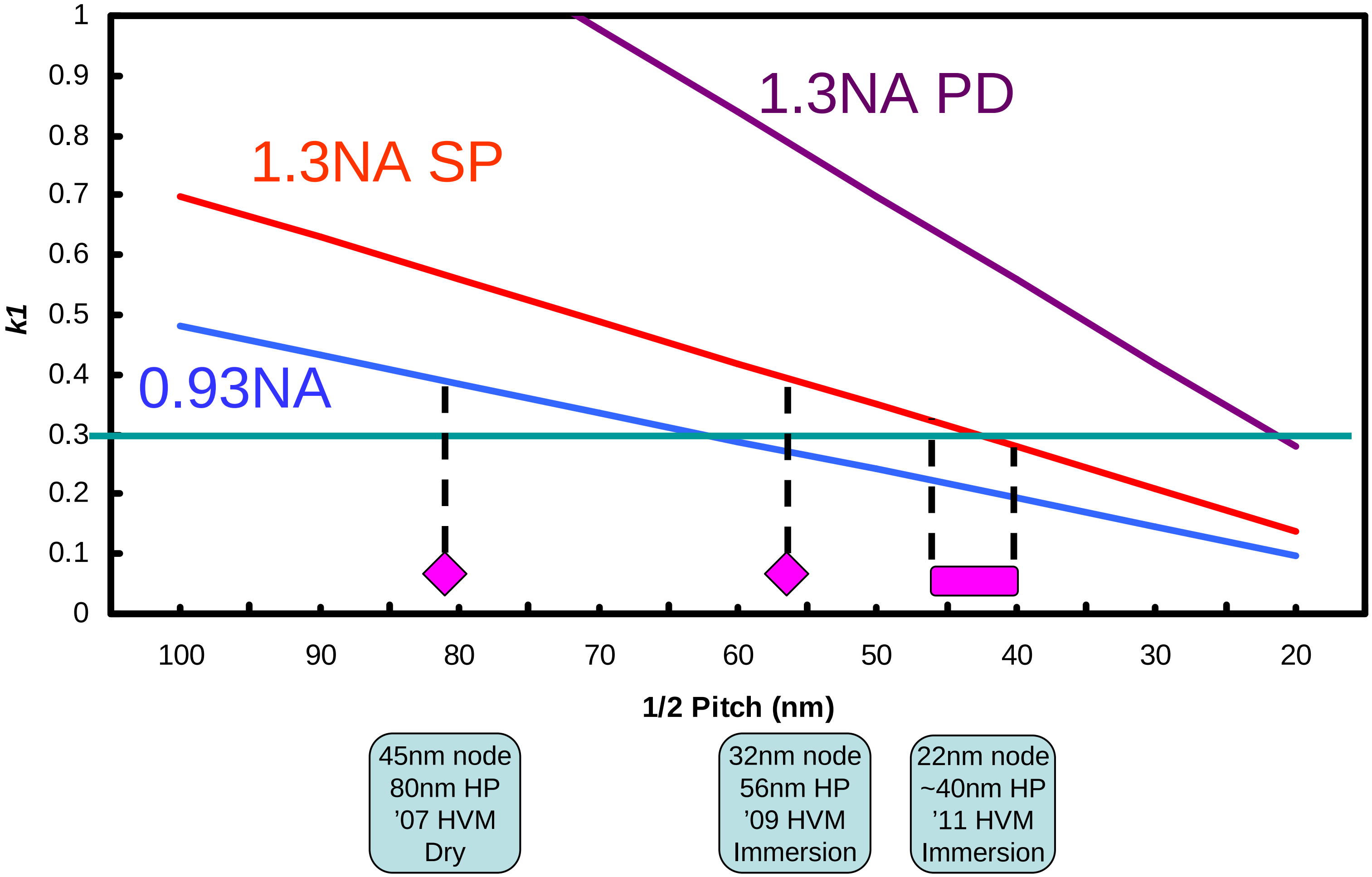
Paths to Feature Size Scaling

$$d = k_1 \frac{\lambda}{NA}$$



- Increase NA
- Enable reduced pitches through process options (like double patterning)
- Reduce Wavelength
- $k_1 < 0.3$ tends to have manufacturability issues

Resolution vs. Technology Roadmap



45nm node
80nm HP
’07 HVM
Dry

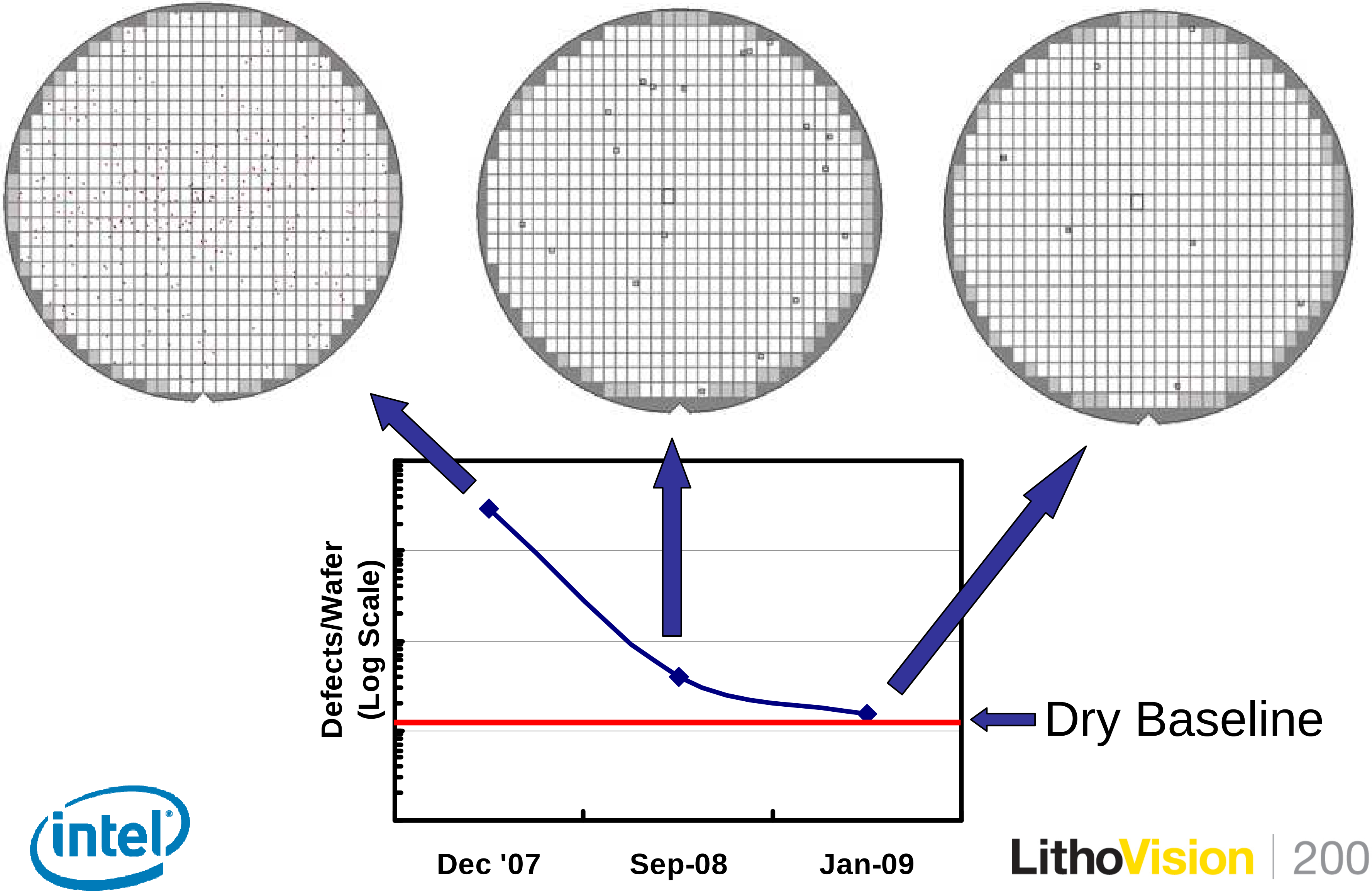
32nm node
56nm HP
’09 HVM
Immersion

22nm node
~40nm HP
’11 HVM
Immersion

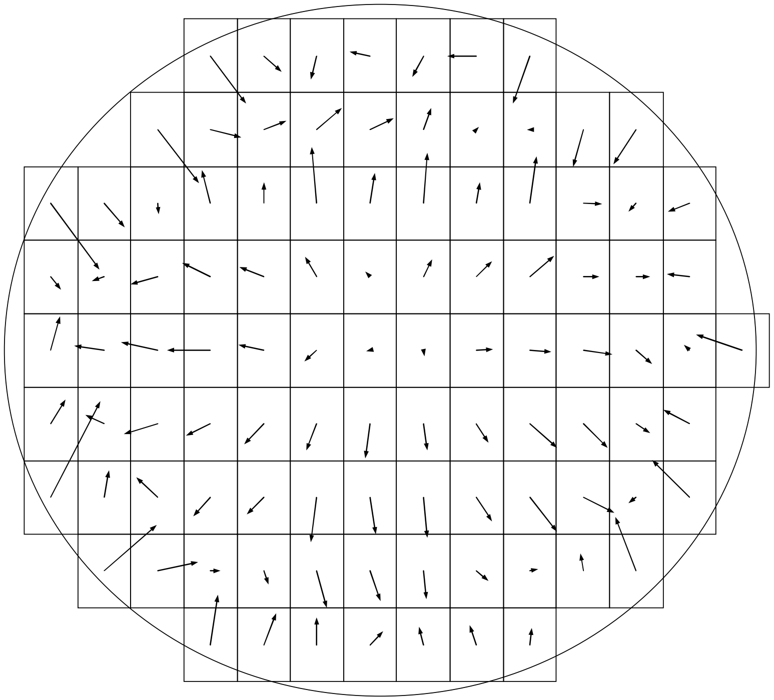
32nm - Immersion Challenges

- Immersion lithography has been a story of steady progress on multiple fronts
  - Basic platform integration and learning
  - Tool stability and operation
  - Defectivity
  - Overlay
- As indicated in 2008 IEDM, Intel's 32nm technology is well on its way to production status
  - Development phase completed
  - Production readiness expected in H2'09
  - Key immersion focus is on platform stability and integration

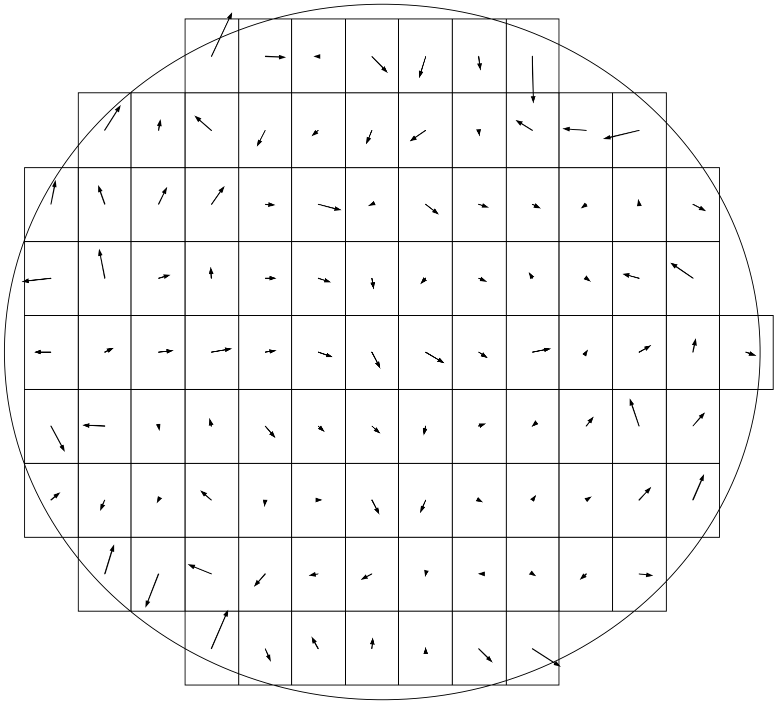
32nm - Immersion Defectivity



32nm – Immersion Overlay



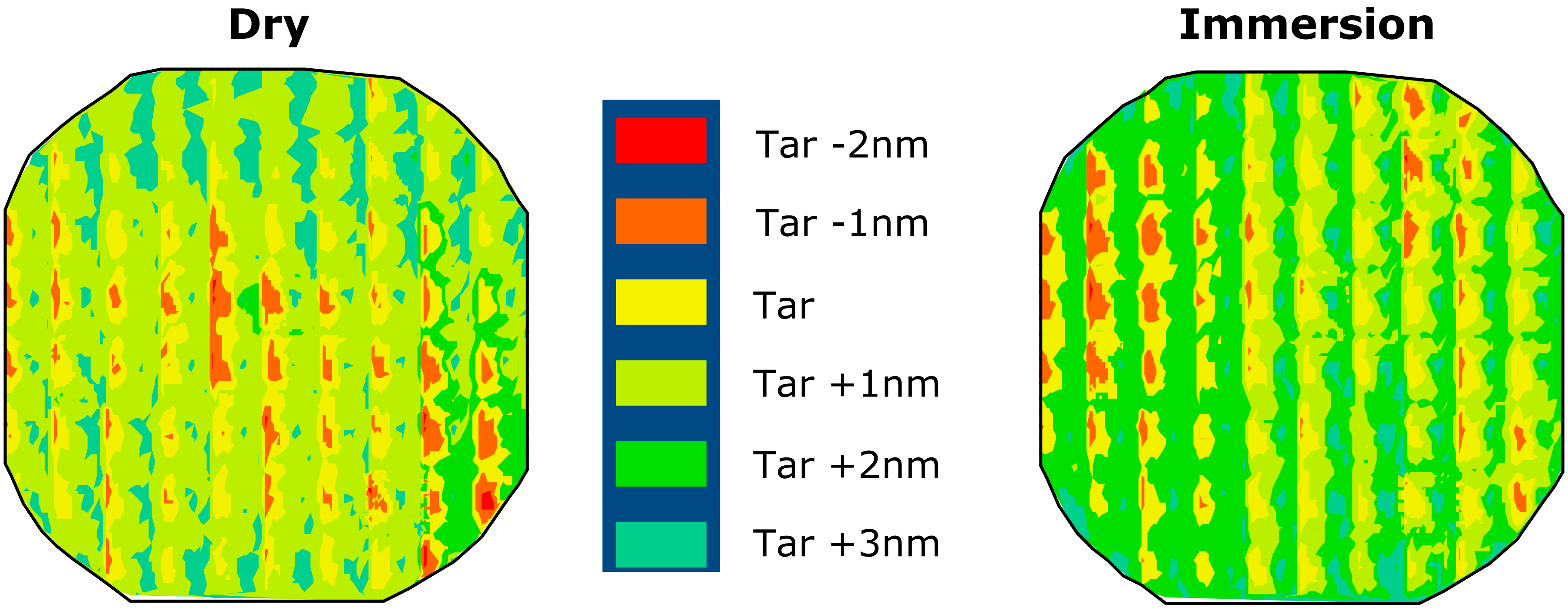
Early Results



Recent Results

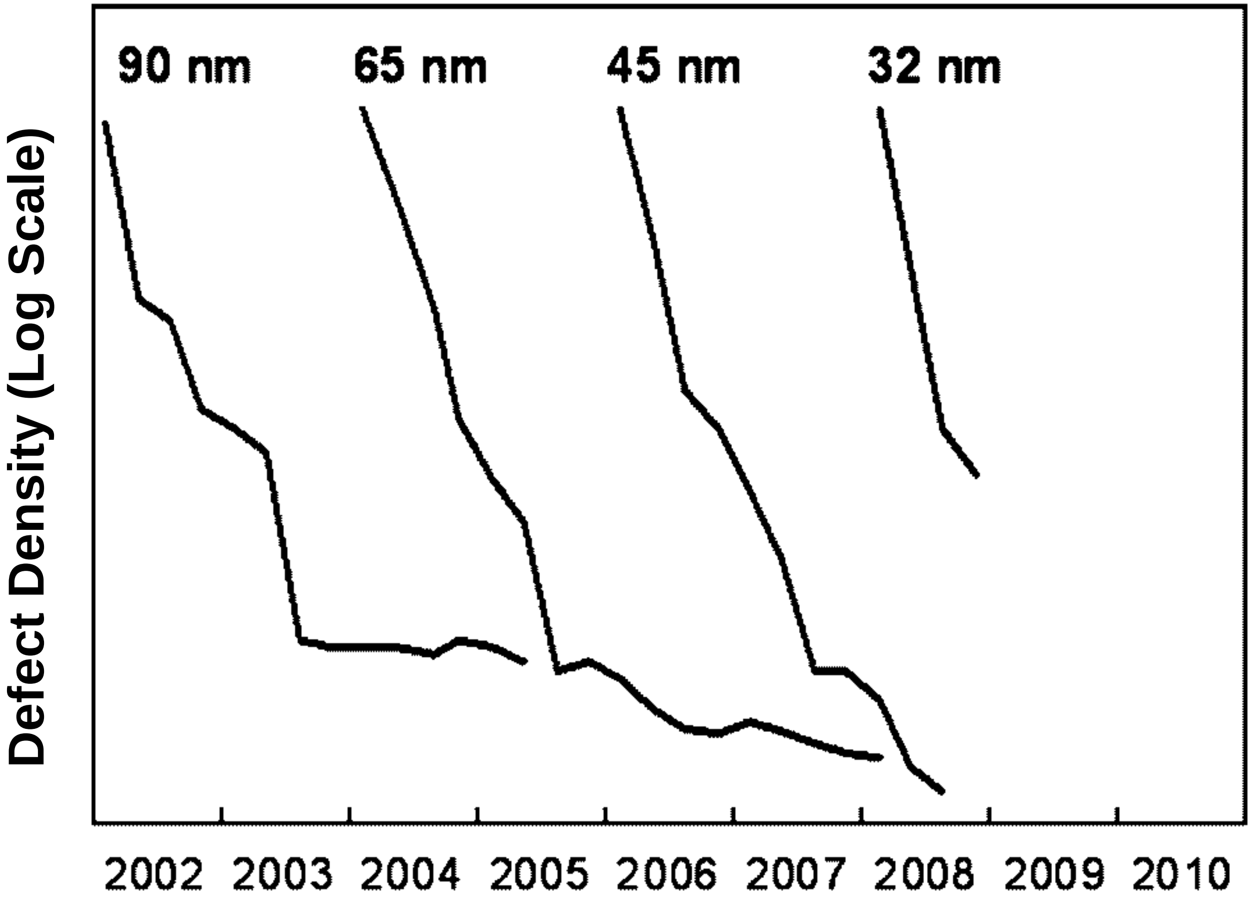
- Significant learning on thermal, focus and alignment effects especially at wafer edge has made wet-dry overlay roughly equivalent to dry-dry

32nm – CD Control



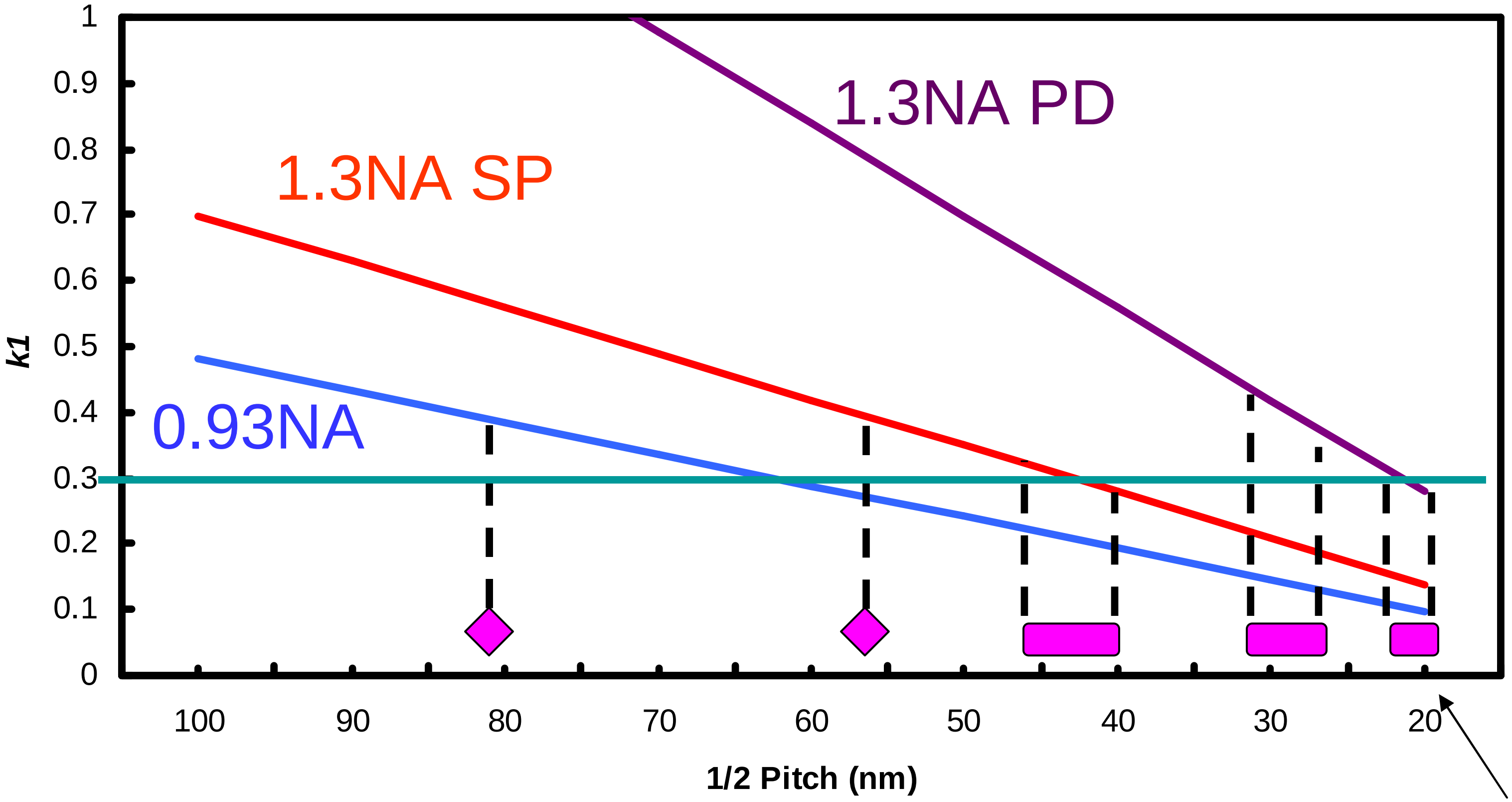
Immersion does not degrade CD uniformity

32nm – Patterning Summary



Immersion litho well on the way to achieving yield parity with dry litho

Resolution vs. Technology Roadmap



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15nm node
26-30nm HP
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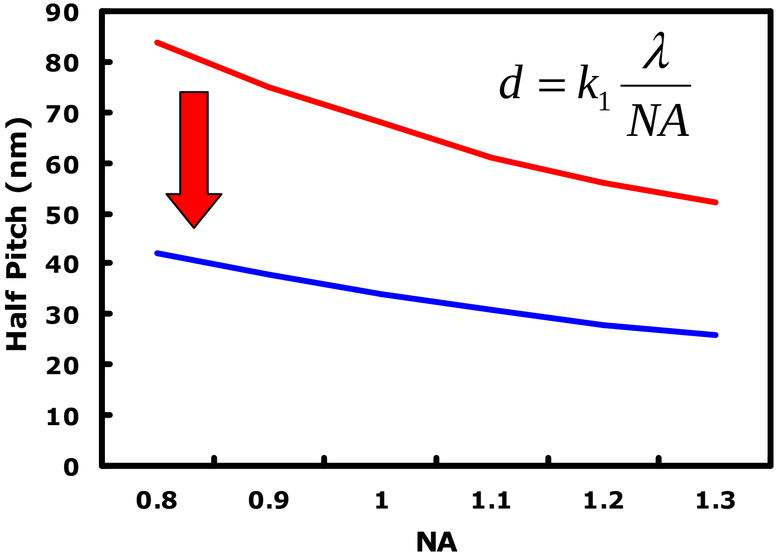
ArF PD/ EUV

11nm node
18-22nm HP
’15 HVM
ArF PD/EUV

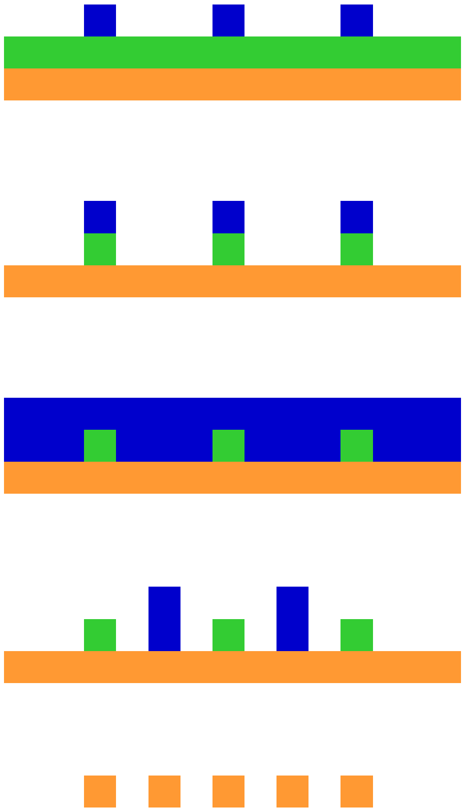
ArF Pitch Division (PD)



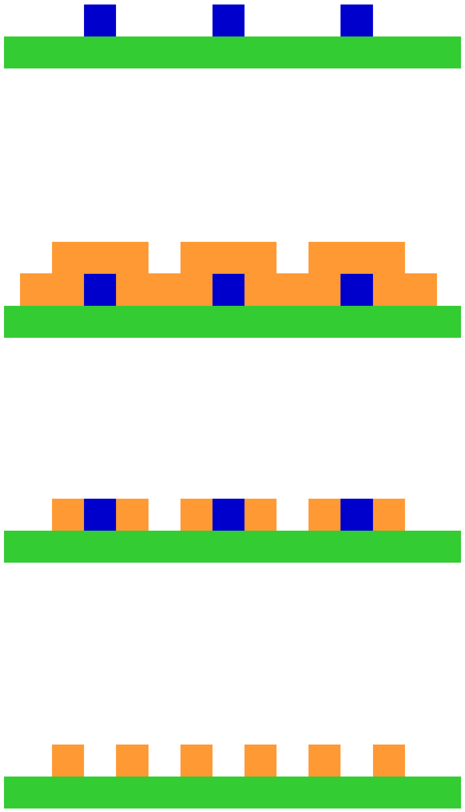
$$d = k_1 \frac{\lambda}{NA}$$

ArF PD gains significant resolution at the expense of process complexity

Double Patterning Pitch Division (DPPD)



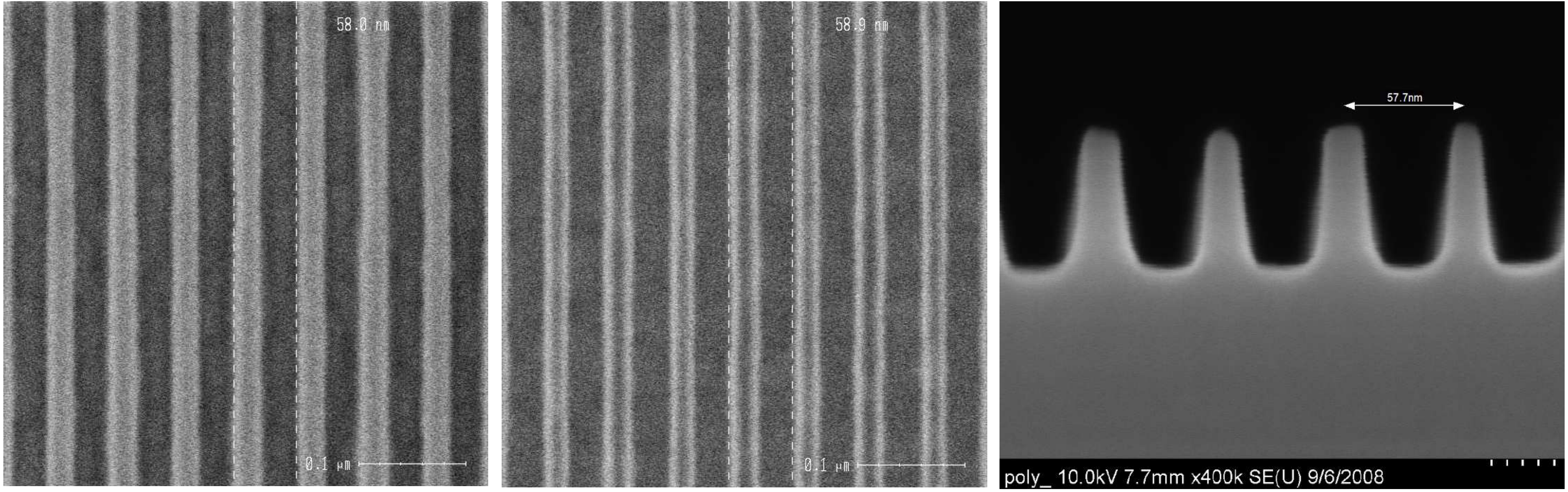
Spacer Based Pitch Division (SBPD)



Double Patterning Pitch Division

- Most mature double patterning methods are either LELE (Litho/Etch/Litho/Etch) or LFLE (Litho/Freeze/Litho/Etch)
  - Line DP can be either. Space DP has to be LELE
- Key challenges are process complexity and synthesis issues in splitting original pattern into two masks

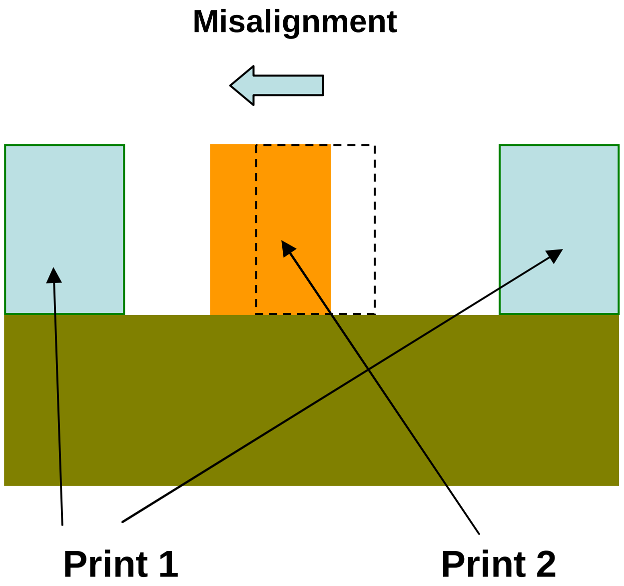
LFLE

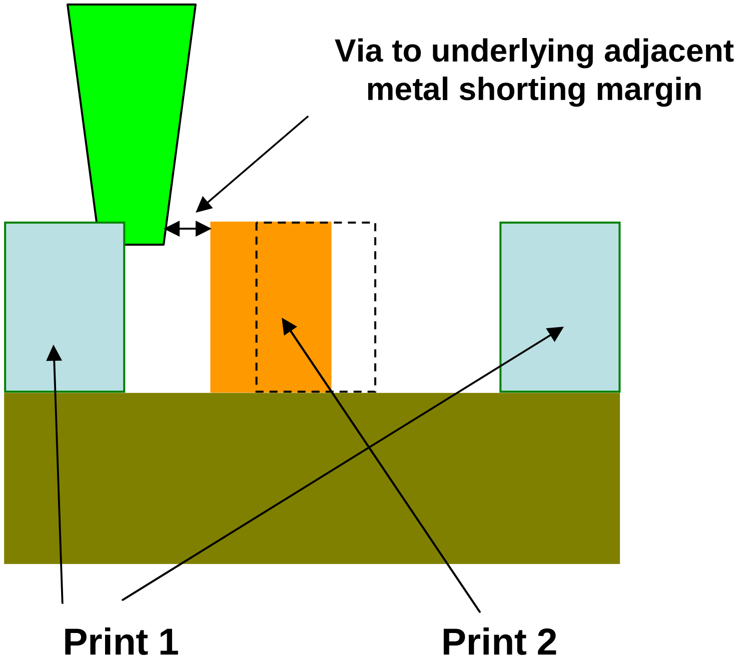


Lithography - DP **Transfer to HM** **Transfer to Substrate**

Double Patterning Disadvantages

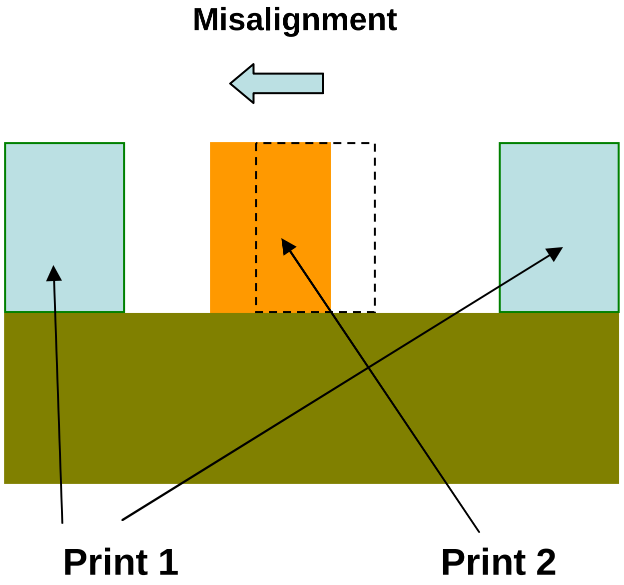
- Misalignment between the 2 exposures is a crucial liability for this technique and can limit its usability
- Interconnect design rule density is critically dependent on shorting margin between vias and adjacent metal lines

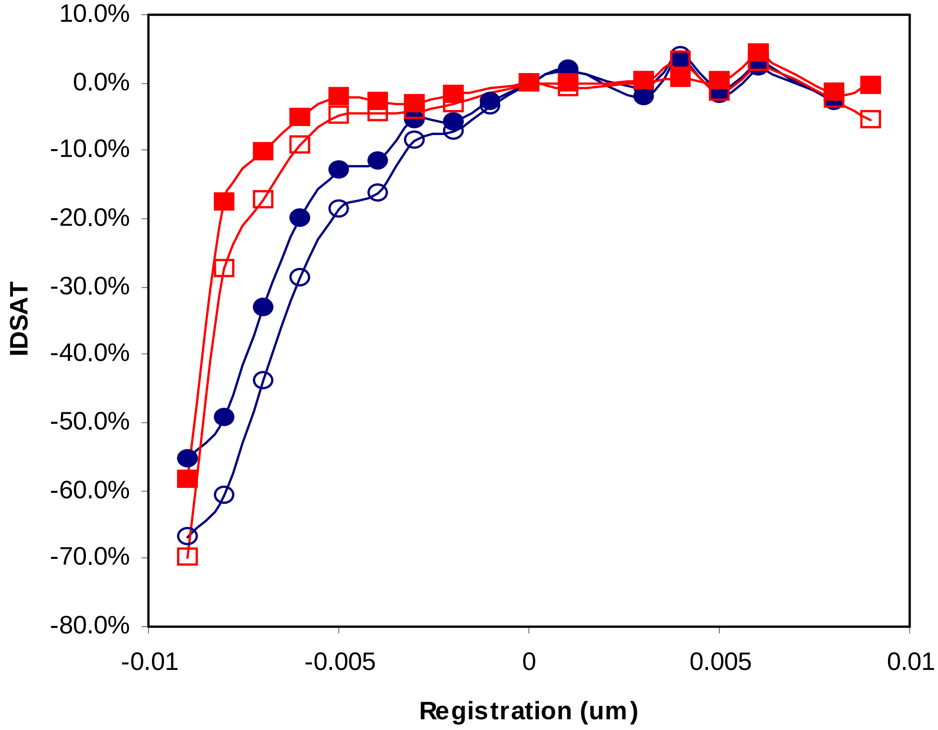




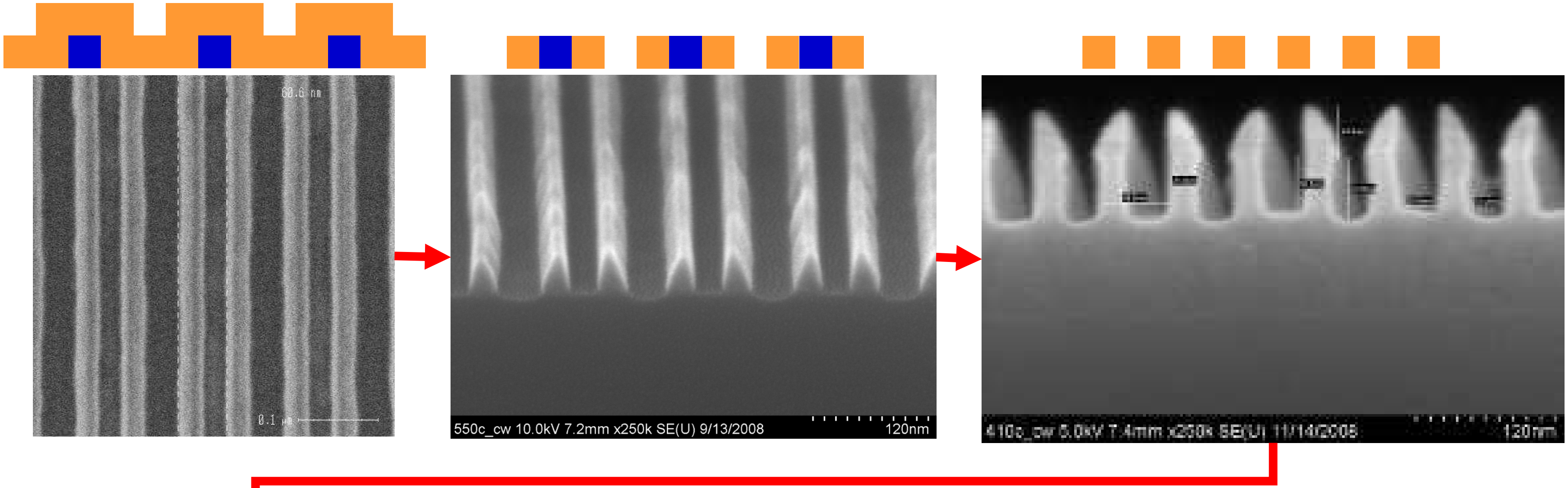
Double Patterning Disadvantages

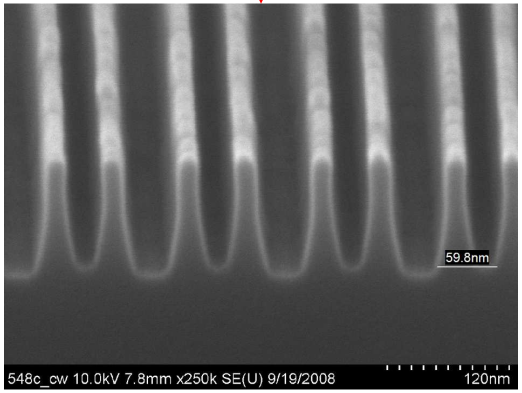
- Misalignment between the 2 exposures is a crucial liability for this technique and can limit its usability
- Transistor parameters can be affected by asymmetry between the source and drain regions





Spacer Based Pitch Division (SBPD)





- SBPD trades off litho complexity (additional masks) for process complexity
- Process demonstrated and reasonable from integration standpoint

Spacer Based Pitch Divison

Disadvantages:

- Can only do one feature size or one space – difficult for random layouts
- Requires trim mask that could be complicated for random layouts

Advantages:

- Edge placement goes (approximately) as ∆CD/2 – can be much more accurate than overlay especially for patterning techniques like APSM
- Likely to require fewer masks even with trim requirement

EUV Tools

- Significant progress being made by scanner suppliers on EUV tool development
- EUV source suppliers are working on higher power sources
- Photoresists have shown significant improvement for resolution, sensitivity and LWR
- Learning relevant to HVM systems will occur in 2009

EUV Litho - Key Gaps

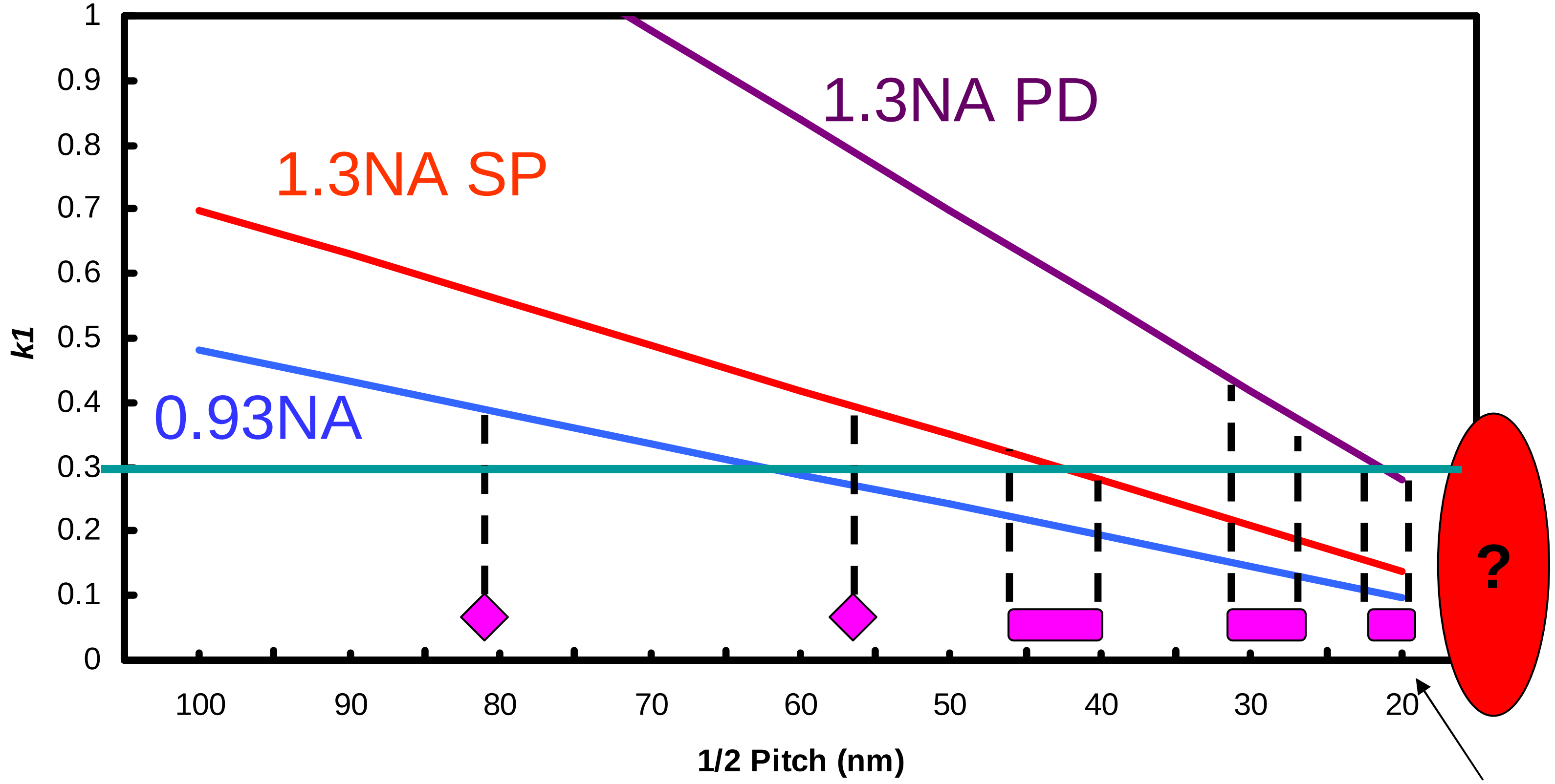
1. Source readiness: funded by suppliers
2. Zero defect reticle process capability: funded by Intel and is 2009 internal focus
3. EUV AIMS and 3G blank inspection: not funded (cost ~ $150M full industry enabling cost)
4. Blank defect improvement trend: insufficiently funded by suppliers (cost is unknown ~ $50M)
5. Fab reticle quality control infrastructure: not funded (cost ~ $10M for single tool)

Technical gaps, especially on the mask defectivity and inspection fronts, will limit EUV HVM insertion if not addressed in time

EUV vs. ArF Pitch Division

- Technical path for ArF Pitch Division (PD) is clear
  - Two paths: DP (LFLE/LELE) or SBPD
  - Both paths are technically straightforward with clear cost structure and advantages/disadvantages – particular choice will be application-specific
- EUV continues to make technical progress but has many challenges
  - Tool integration is a significant challenge
  - Source power gap needs to be closed
  - Photoresists need further improvement
  - Key technical gap is in the area of mask defect inspection
- Decision between ArF PD and EUV will be made for 15nm node (26-30nm HP) based on
  - EUV scanner and supporting infrastructure readiness vs. 2013 HVM need
  - COO of EUV vs. ArF PD

Resolution vs. Technology Roadmap



45nm node 80nm HP ’07 HVM Dry	32nm node 56nm HP ’09 HVM Immersion	22nm node ~40nm HP ’11 HVM Immersion	15nm node 26-30nm HP ’13 HVM ArF PD/ EUV	11nm node 18-22nm HP ’15 HVM ArF PD/EUV

No simple ArF PD Solution below ~ 20nm HP

Patterning Outlook Summary

- Immersion lithography moving into production phase with equivalent expected quality relative to dry lithography
- Below about 40nm HP, SE ArF lithography does not have adequate process latitude - ArF PD expected to deliver patterning capability
- EUV introduction dictated entirely by readiness of key technology elements and COO relative to ArF PD
  - Serious gaps exist on mask and inspection fronts
  - May be in time for 15nm node (26-30nm HP) HVM if technical issues are resolved
- No simple ArF Pitch Division solution exists below about 20nm HP (11nm node)
  - Would the solution be EUV or other ArF extensions like Spacer Based Pitch Quadrupling?
  - How can the solution be made affordable?

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Thank You!!