LithoVision | 2008

Current Status of Immersion Lithography for NAND/CMOS Device

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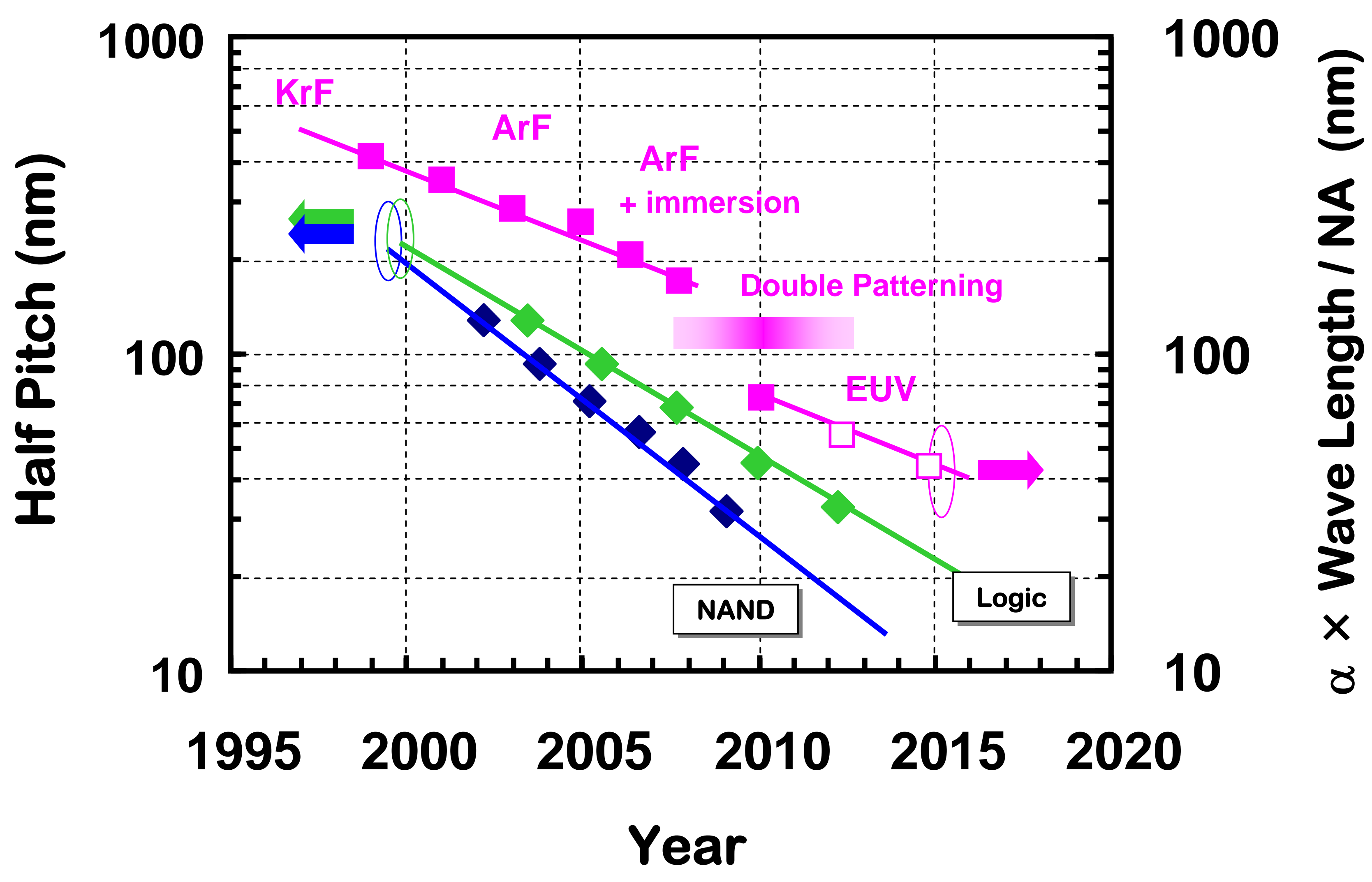
Toshiba Corporation

Outline

- Lithography History & Future
- Current Status of Immersion Lithography
- HP 32 nm generation and beyond
- Summary

Lithography History & Future



Lithography Roadmap for ArF

From Single to Double

Half Pitch : HP (nm)

140
120
100
80
60
40
20

0.6 0.8 1 1.2 1.4 1.6 1.8

NA

Logic

Line

Hole

NAND

$$HP = k_1 \times \frac{\lambda_0}{NA}$$

k_1

0.50
0.45
0.40
0.35
0.30
0.25

	NAND	Logic	
Level / HP[nm]		LS	CH
90	SE	SE	SE
65-70	SE	SE	SE
55	SE	-	-
45	SE	SE	DP
32-	DP	DP	DP

SE : Single Exposure
DP : Double Patterning

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Logic
Line
Hole
NAND

k_1
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0.45
0.40
0.35
0.30
0.25

Nikon
S609B
NA1.07

Nikon
S610C
NA1.30

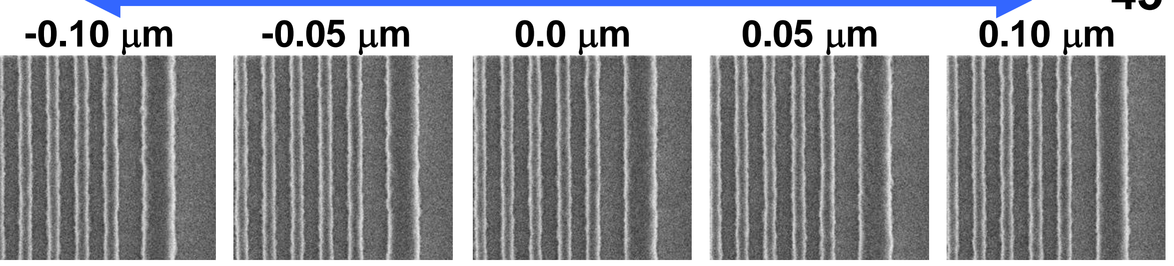
55 nm NAND, 45 nm Node Logic Lithography

S609B installed in Toshiba at 2006/B.

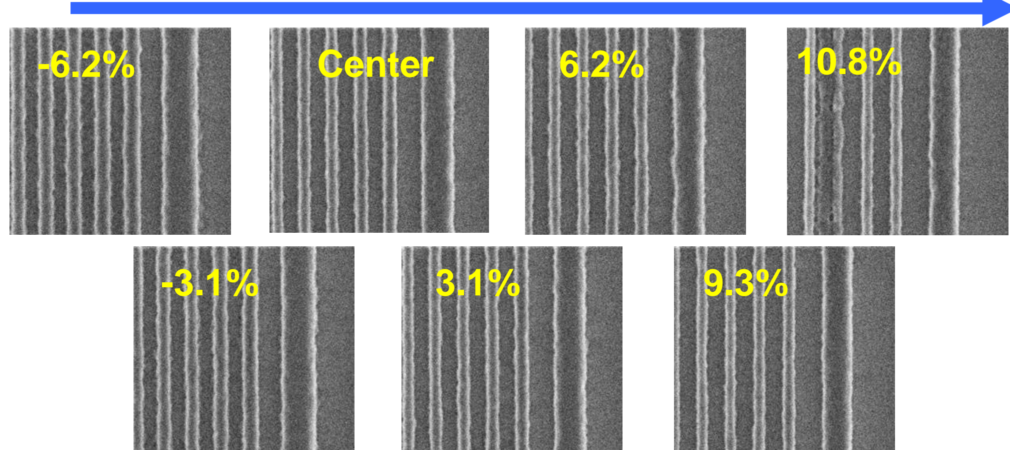
HP 55 nm NAND

■Focus Latitude

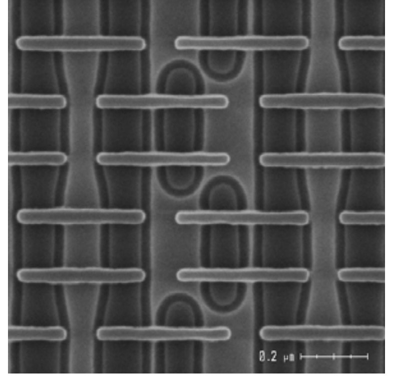
Range : 0.20 μm



■Dose Latitude



45 nm node (HP 65 nm) Logic



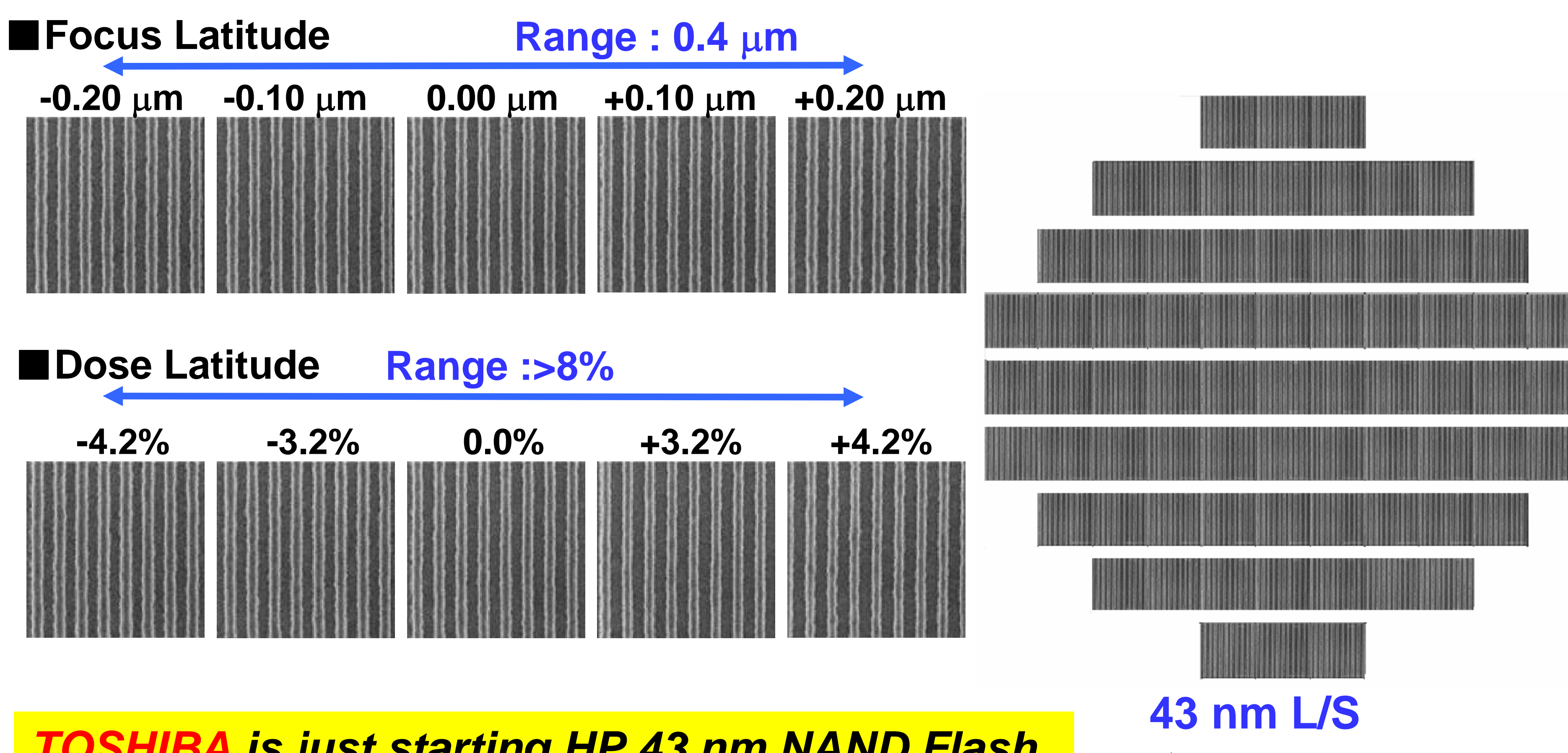
TOSHIBA has started HP 55 nm NAND Flash production using NIKON S609B scanners!

NIKON S610C NA 1.30 Immersion Exposure Tool

S610C installed in Toshiba at 2007/B.

CD-Control/ED-Margin of HP 43 nm NAND Flash Pattern

Exposure: Nikon S610C (NA=1.30, Crosspole & Polarized illumination)
Resist: Optimized ArF Immersion Resist with Top Coat



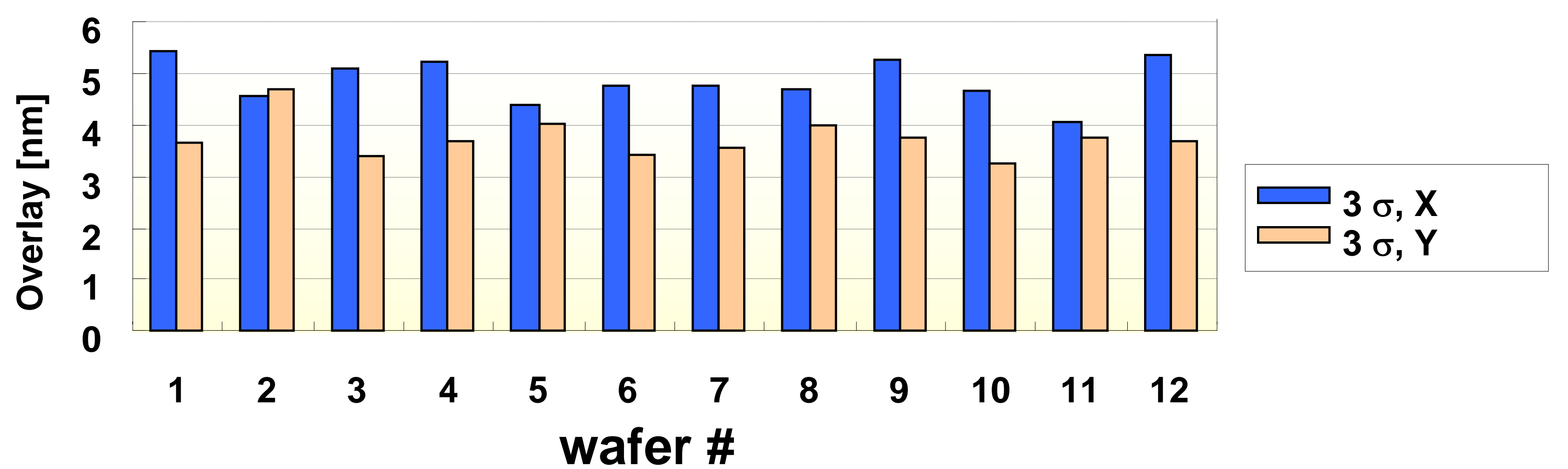
TOSHIBA is just starting HP 43 nm NAND Flash production using NIKON S610C scanners!

Immersion-specific Challenges

Immersion-specific Challenges

- Heat of Water Evaporation
  - Overlay Accuracy
  - Focus Accuracy
- Water Induced Defect Control
  - Meniscus Control
    - Bubble
    - Water Droplet Water Mark → Stain
  - Leaching Control
    - Stain
  - Wafer Edge Control
    - Particles
    - Film Peeling

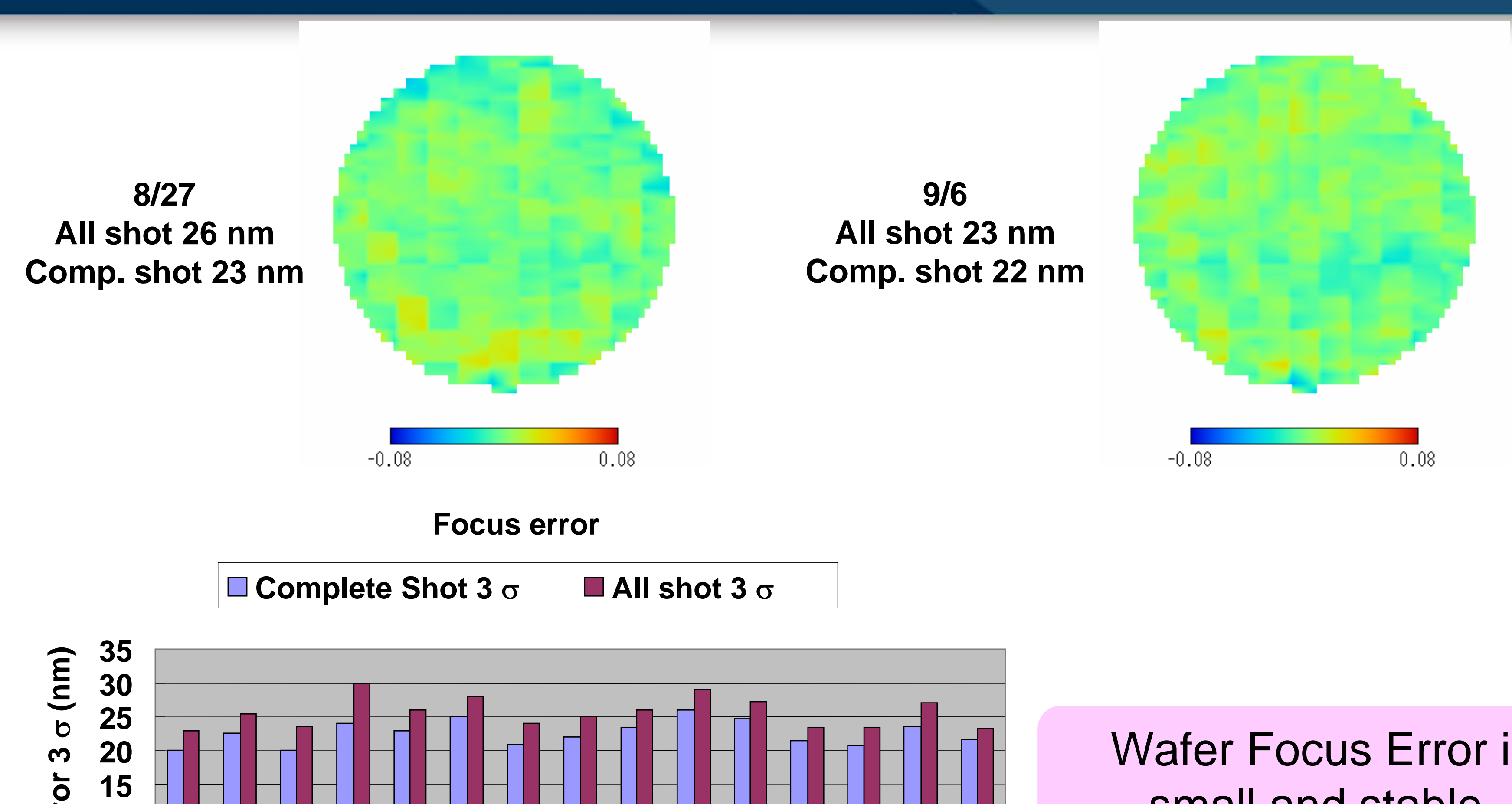
S610C Single Machine Overlay



	X (nm)	Y (nm)
Overlay (3σ)	4.8	3.7

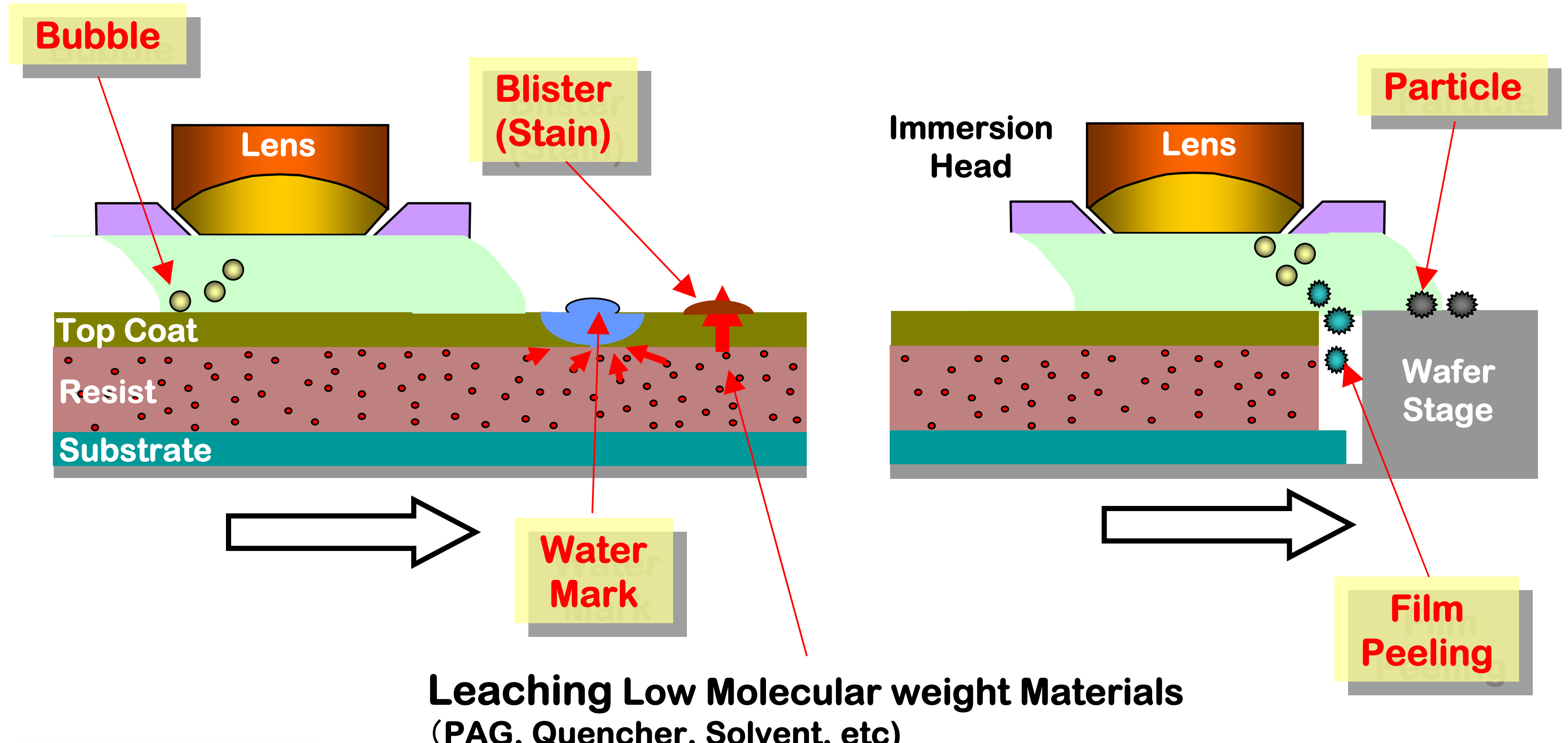
● The results are small enough for HP 40-45 nm feature.

S610C Focus Accuracy Stability



Wafer Focus Error is small and stable.

Risks for Immersion Defect Sources



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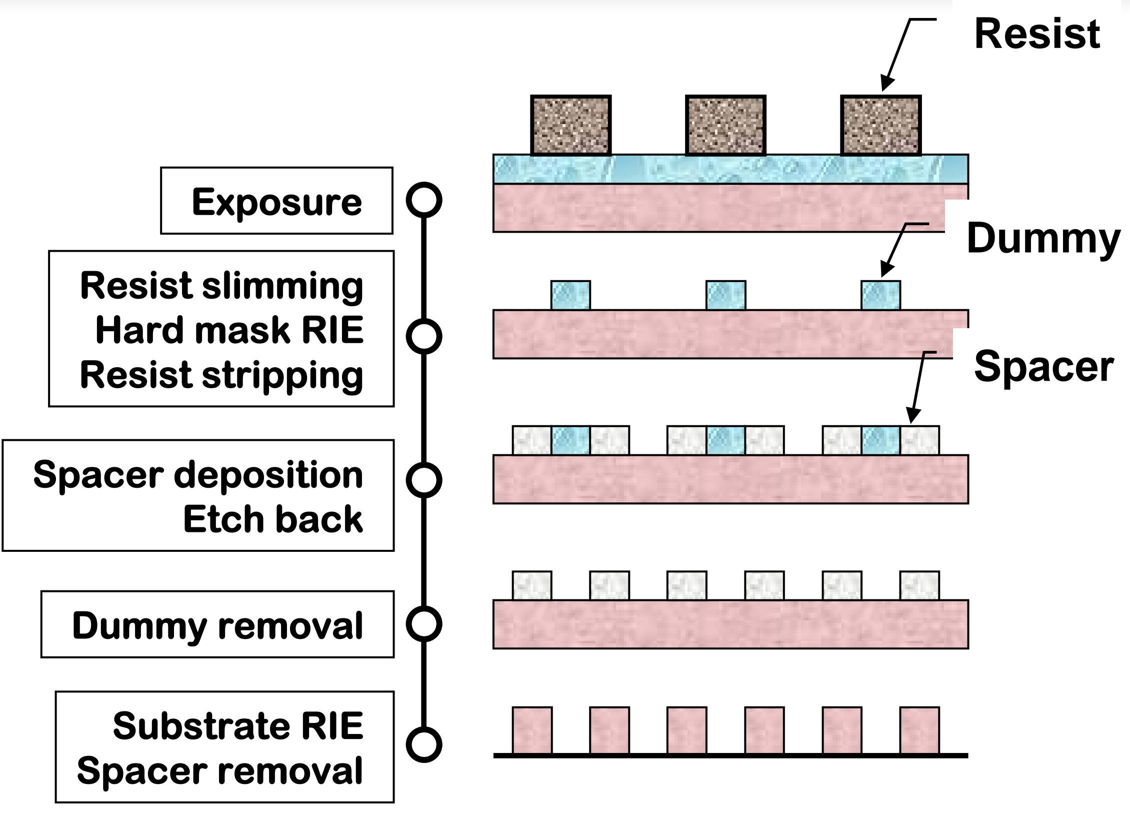
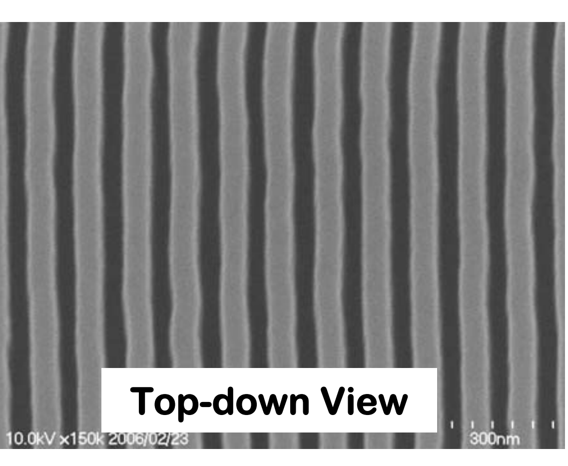
Double Patterning Process

1 Dimension (k1 < 0.25)

Pitch Splitting		Edge Patterning	
Dark Field 3:1	Bright Field 1:3	Spacer Process	Double Development

Spacer Process





T1MS-4511-02 B4-1

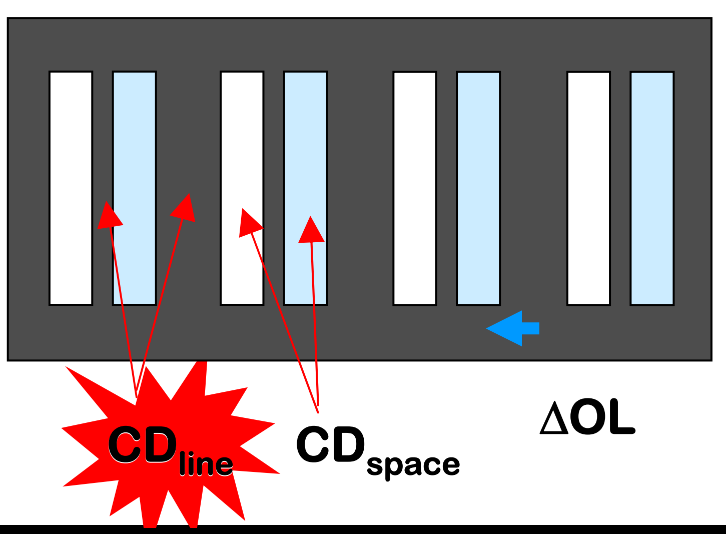
Cross-section View

- Suitable for Periodic Structure ☺
- Complicated and Long Process ☹
- Cost Issue ☹

TOSHIBA

CD Control for Pitch Splitting

ΔCD Budget



ΔCD budget [%]		ΔCD_{Line} [%]	ΔCD_{Space} [%]
Litho ΔCD		10.0	10.0
Etching ΔCD		8.0	8.0
Overlay induced ΔCD	Mask IP	1.5	0.0
	Scanner	5.6	0.0
	Process	5.0	0.0
	Total	7.7	0.0
		14.9	12.8

Summary

- Lithography roadmap for NAND and Logic has made clear.
- 55 nm NAND Flash and 45 nm node (HP 65nm) logic immersion process had been developed using S609B (NA>1.0)
- The litho. Process for 43 nm NAND Flash and 32 nm node (HP 45nm) logic have been successfully developed with Nikon S610C.
- Immersion lithography has been matured technology for HP 55-45nm devices.
- Further improvements, i.e. defectivity and throughput, are necessary for improving productivity.
- For HP 3X nm and beyond, double patterning (DP) technologies , such as spacer process and pitch splitting, will become promising candidates. Further improvement of overlay is necessary for pitch splitting.

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Thank you !